Sitronix

ST5625CA

6-Bit 1200-Channel TFT LCD Source Driver with TCON

Product Description

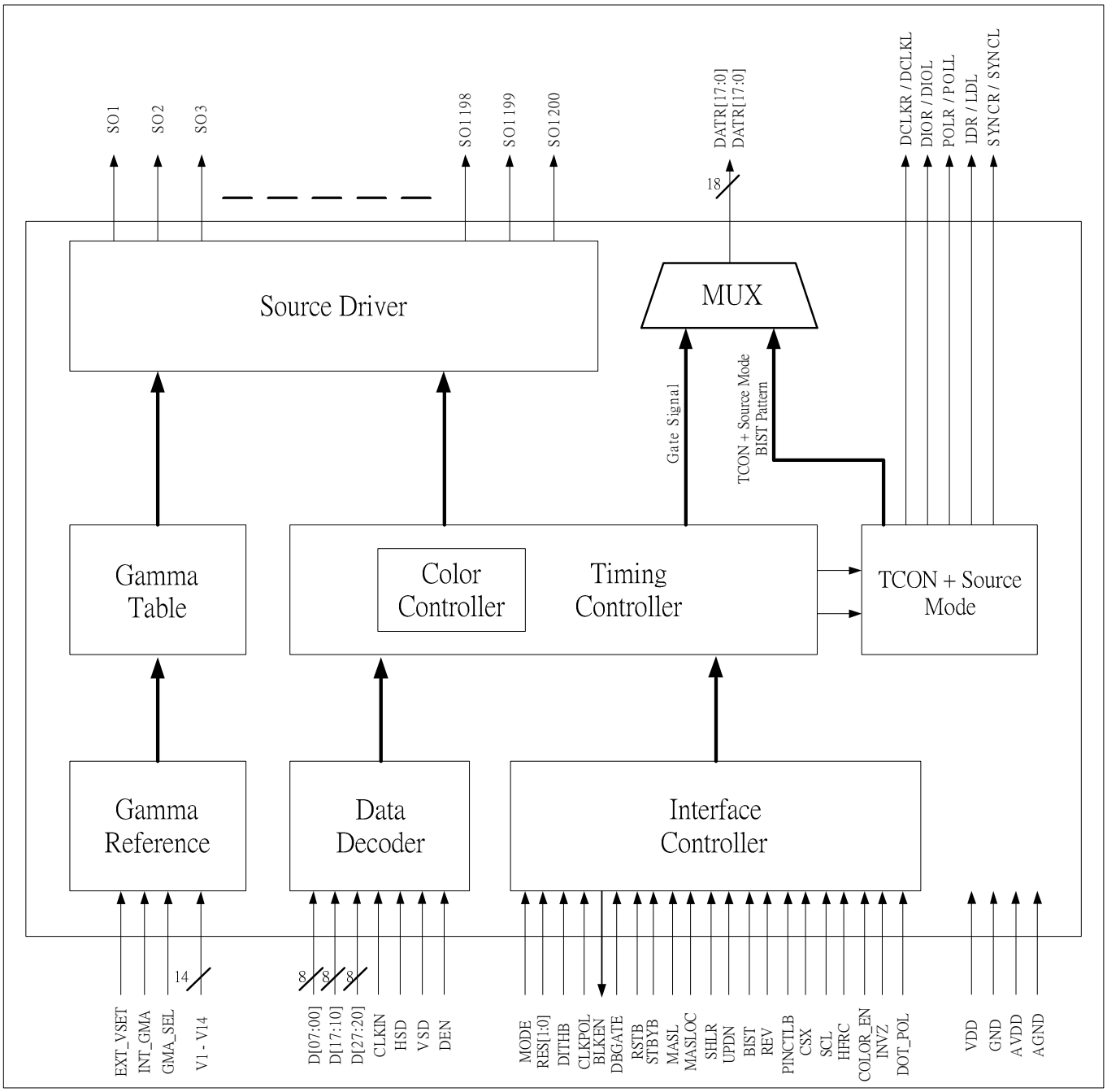
ST5625CA is a highly integrated 1200 channel source driver with TTL interface Timing Controller for color TFT-LCD panels. ST5625CA integrate source driver, timing controller and pin control interface. Input data can support TTL digital 18-bit / 24-bit parallel RGB data format, and source driver support 256 gray scales with dithering features. All functions can be set by relative H/W pin.

ST5625CA support two chip operation T-con + Source mode. Configurable Master and Slave configuration increase the flexibility for different panel design. With wide range of supply voltages and small output deviations make this chip more suitable for various applications.

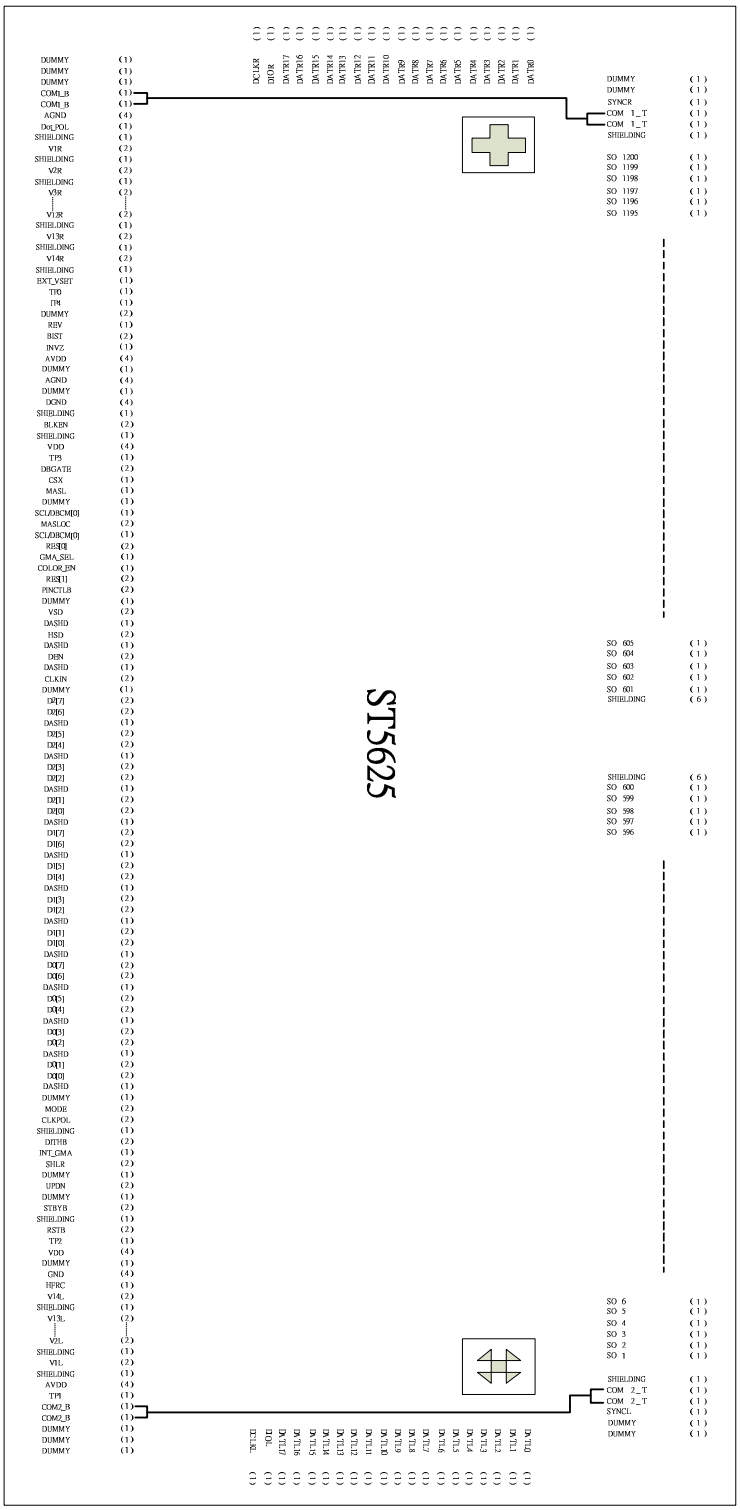
Features

- A color TFT LCD source drivers with timing controller
- Supports TTL 18-bit or 24-bit parallel (RGB) input timing
- Output : 1200 output channels
- Supports four type resolutions : 800(RGB)x600、800(RGB)x480、640(RGB)x480、400(RGB)x240
- 8-bit resolution 256 gray scales with 2-bits dithering (L/HFRC)
- Support single or dual-gate operation mode
- Support T-con data mapping Z & Inv. Z type at dual gate mode
- Support to configure Color function via 3-line SPI mode
- Support stand-by mode for low power consumption
- Support dot inversion driving scheme
- Support External Gamma buffer (10/14 Gamma)
- Built-in Color function
- Built-in Internal Gamma ratio
- Power of LCD driving voltage : 6.5 ~ 13.5V
- Output dynamic range : 0.1 ~ AVDD-0.1V
- Power for logic circuit : 2.7V~3.6V
- Operating frequency : 50MHz
- Output deviation : ± 20mV
- Package : COG available

Function Block Diagram



Pin Assignments (Bump View)



Pin Description

Designation	I/O	Default	Description
D07~D00 D17~D10 D27~D20	I	-	Parallel data Input. For TTL 24-bit parallel RGB image data input. D07~D00 = R[7:0] data; D17~D10= G[7:0] data; D27~D20 = B[7:0] data. For 18bit RGB interface, connect two LSB bits of all the R/G/B data buses to GND.
CLKIN	I	-	Clock for Input Data. Data latched at rising/falling edge of this signal. Default falling edge.
HSD	I	High	Horizontal Sync input. Negative polarity. Normally pull high. For DE mode application , Connect HSD pin to VDD
VSD	I	High	Vertical Sync input. Negative polarity. Normally pull high. For DE mode application , Connect VSD pin to VDD
DEN	I	Low	Data Input Enable. Active High to enable the data input bus under “DE Mode”. Normally pull low. For SYNC mode application , Connect DEN pin to GND
MODE	I	High	DE / SYNC mode select. Normally pull high. MODE = ”H” : DE mode. (Default) MODE = ”L”: HSD/VSD mode.
RES[1:0]	I	Low	Display resolution selection. Normally pull low. RES[1:0] = "LL" , for 800(RGB)*480 display resolution.(Default) RES[1:0] = "LH" , for 800(RGB)*600 display resolution. RES[1:0] = "HL" , for 640(RGB)*480 display resolution. RES[1:0] = "HH" , for 400(RGB)*240 display resolution. Note: When RES[1:0]="HL" , channel 481~720 is disable
DITHB	I	High	Dithering function enable control. Normally pull high DITHB = "H", Disable internal dithering function.(Default) DITHB = "L", Enable internal dithering function.
CLKPOL	I	Low	Input clock edge selection. Normally pull low. CLKPOL = "H", Latch data at CLKIN rising edge. CLKPOL = "L", Latch data at CLKIN falling edge. (Default)
BLKEN	O	-	Backlight enable control signal for external controller. BLKEN = "H", Logical control signal to turn on external backlight controller. BLKEN = "L", Turn off external backlight controller. Note: Refer to the Power On/Off Sequence for the detail information.
DBGATE	I	Low	Dual Gate function enables control. Normally pull low. DBGATE = "H" , Enable Dual Gate Function. DBGATE = "L" , Disable Dual Gate Function (Default)
V1 ~ V14	I	-	Gamma correction reference voltage. These input voltage must be supplied by user. Case1 : EXT_VSET="L" AGND+0.1<V14<V12<V11<V10<V8;V7<V5<V4<V3<V1< AVDD-0.1 V2, V6, V9, V13 pads are disabled. Case2 : EXT_VSET="H" AGND+0.1<V14<V13<V12<V11<V10<V9<V8;V7<V6<V5<V4<V3<V2<V1< AVDD-0.1
RSTB	I	High	Global reset pin. Active Low to enter Reset State. Suggest to connecting with an RC reset circuit for stability. Normally pull high.
STBYB	I	High	Standby mode, Normally pull high. STBYB ="H", normal operation(Default) STBYB ="L", timing controller, source driver will turn off, all output are High-Z
MASL	I	High	Master and Slave Mode selection. Normally pull high. MASL = "H", for Master mode. (Default Mode) MASL = "L", for Slave mode. Only the Master chip will issue the Gatel.

MASLOC	I	Low	Master location definition pin. Normally pull low. MASLOC = "L", Master locate on right side (Panel top view). (Default Mode) MASLOC = "H", Master locate on left side (Panel top view).
SHLR	O	High	Source Right or Left sequence control. Normally pull high. SHLR = "L", shift left: last data = S1←S2←S3.....←S1200 = first data. SHLR = "H", shift right: first data = S1→S2→S3.....→S1200 = last data.(Default)
UPDN	I	Low	Gate Up or Down scan control. Normally pull low. UPDN = "L", STV2 output vertical start pulse and UD pin output logical “0” to Gate driver.(Default) UPDN = "H", STV1 output vertical start pulse and UD pin output logical “1” to Gate driver.
BIST	I	Low	Normal Operation/BIST pattern select. Normally pull low. BIST = "H" : BIST(DCLK input is not needed) BIST = "L" : Normal Operation
REV	I	Low	Data inverted control. Normally pull low. REV="H" : Data inverted for normally black LCD REV="L" : Data not inverted for normally white LCD. (Default)
PINCTL	I	High	Enable hardware pin control function. Normal pull high. PINCTL="H" , Enable hardware pin control. (HW > SW) PINCTL="L", Enable software control by 3-wire SPI interface. (SW > HW)
CSX	I	High	Serial communication chip select. Normally pull high. When CSX=”L” , 3-wire SPI mode, When CSX=”H” , Color Enhance selection mode.
SCL/DBCM[0]	I	High	Multi-Function Selection: Normally pull high. When CSX="L" , this pin act as 3-wire "SCL / SDA" pin. When CSX="H" , this pin act as Color Enhance mode select pin (bit0)
SDA/DBCM[1]	I/O	High	Multi-Function Selection: Normally pull high. When CSX="L" , this pin act as 3-wire "SCL / SDA" pin. When CSX="H" , this pin act as Color Enhance mode select pin (bit1)
HFRC	I	High	H-FRC selection(needs dithering function enable). Normally pull high. HFRC=H : H-FRC HFRC=L : L-FRC
COLOR_ENB	I	Low	Color Enhance function select pin. Normally pull low. COLON_ENB = "H" , Disable color enhance function. COLON_ENB = "L" , Enable color enhance function.
INVZ	I	Low	INVZ Type selection. (Only for dual gate mode). Normally pull low. INVZ. = "H" , 1st Gate output start at "R" pixel. (Z inv.) INVZ = "L" , 1st Gate output start at "G" pixel. (反 Z inv.)
INT_GMA	I	High	Internal Gamma enable. Normally pull high. INT_GMA = "L" , Disable Internal Gamma INT_GMA = "H" , Enable Internal Gamma
GMA_SEL	I	Low	Gamma curve select pin. Normally pull low. GMA_SEL = "L" , 1st panel Gamma curve. GMA_SEL = "H", 2nd panel Gamma curve.
EXT_VSET		Low	10/14 External Gamma selection. Normal pull low. EXT_VSET = "L" , External 10 Gamma EXT_VSET = "H" , External 14 Gamma
Dot_POL		High	Dot Polarity Inversion. (Only for dual gate mode). Normal pull high. Dot_POL = "H" , 1+2-dot Inversion Dot_POL = "L" , 2-dot Inversion

DATR[17:0]	I/O	-	Multi function I/O pin. Refer to the Cascade DAT pin mapping table for the detail.
DCLKR	I/O	-	Master and Slave cascade control signal.
DIOR	I/O	-	Master and Slave cascade control signal.
SYNCR	I/O	-	Master and Slave cascade control signal.
DATL[17:0]	I/O	-	Multi function I/O pin. Refer to the Cascade DAT pin mapping table for the detail.
DCLKL	I/O	-	Master and Slave cascade control signal.
LDL	I/O	-	Master and Slave cascade control signal.
SYNCL	I/O	-	Master and Slave cascade control signal.
AVDD	PI	-	Power supply for analog circuits
AGND	PI	-	Ground pins for analog circuits
VDD	PI	-	Power supply for digital circuits
GND	PI	-	Ground pins for digital circuits
SO1~SO1200	O	-	Source Driver Output Signals. All outputs will be of unknown values under stand-by mode.
TP4~0	T	-	Test Pin. Float these pins for normal operation.
ALIGN	M	-	For assembly alignment.
COM1_B COM1_T	S	-	Internal link together between input side and output side.
COM2_B COM2_T	S	-	Internal link together between input side and output side.
SHIELDING	SH	-	IC Shielding pads. Those pins are internally connected to the AGND. DO NOT connect to any WOA on the panel.
DASHD	SH	-	Data Bus Shielding pad. Those pins are internally connected to the GND. RECOMMAND to add shielding lines on the FPC to reduce EMI.
DUM	D	-	Dummy pads. Those pins are floating pads.

Note:
I: Input, O: Output, P: Power, S: Shorted line, PI: Power input, PO: Power output,
T: Testing, SH: Shielding, I / O: Input / Output, D:Dummy.

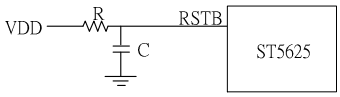
Pass Line Description:

Pass Line No:	**Pad Name**	
1	COM1_B	COM1_T
2	COM2_B	COM2_T

Color Enhance Function Control description:

Color_ENB	PINCTL	CSX	SDA/ DBCM[1]	SCL/ DBCM[0]	Color Function
1	X	X	X	X	CE Disable
0	1	1	0	0	CE setting 0 (Strong)
0	1	1	0	1	CE setting 1 (Middle)
0	1	1	1	0	CE setting 2 (Weakest)
0	1	1	1	1	CE setting 3 (Weak) [Default]

Application Circuit for Reset function



Recommend R =47kΩ, C=0.1uF

Value of wiring resistance to each pin

The recommended wiring resistance values are shown below. The wiring resistance values affect the current capacity of the power supply, so be sure to design using values that do not exceed those recommended.

Pin Name	Wiring Resistance Value(Ω)	Pin Name	Wiring Resistance Value(Ω)	Pin Name	Wiring Resistance Value(Ω)
VDD	< 25	DITHB	< 1K	SDA	< 200
AVDD	< 5	CLKPOL	< 1K	HFRC	< 1K
GND	< 25	DBGATE	< 1K	COLOR_ENB	< 1K
AGND	< 5	RSTB	< 1K	INVZ	< 1K
V1~V14	< 10	STBYB	< 1K	INT_GMA	< 1K
D00~D07	< 200	MASL	< 1K	GMA_SEL	< 1K
D10~D17	< 200	MASLOC	< 1K	EXT_VSET	< 1K
D20~D27	< 200	SHLR	< 1K	Dot_POL	< 1K
CLKIN	< 50	UPDN	< 1K	DATR/L[17:0]	< 200 & 20pf
HSD	< 200	BIST	< 1K	DCLKR/L	< 200 & 20pf
VSD	< 200	REV	< 1K	DIOR/L	< 200 & 20pf
DEN	< 200	PINCTL	< 1K	SYNCR/L	< 200 & 20pf
MODE	< 1K	CSX	< 200		
RES[1:0]	< 1K	SCL	< 200		

DATR[17:0] / DTAL[17:0] pin mapping Table:

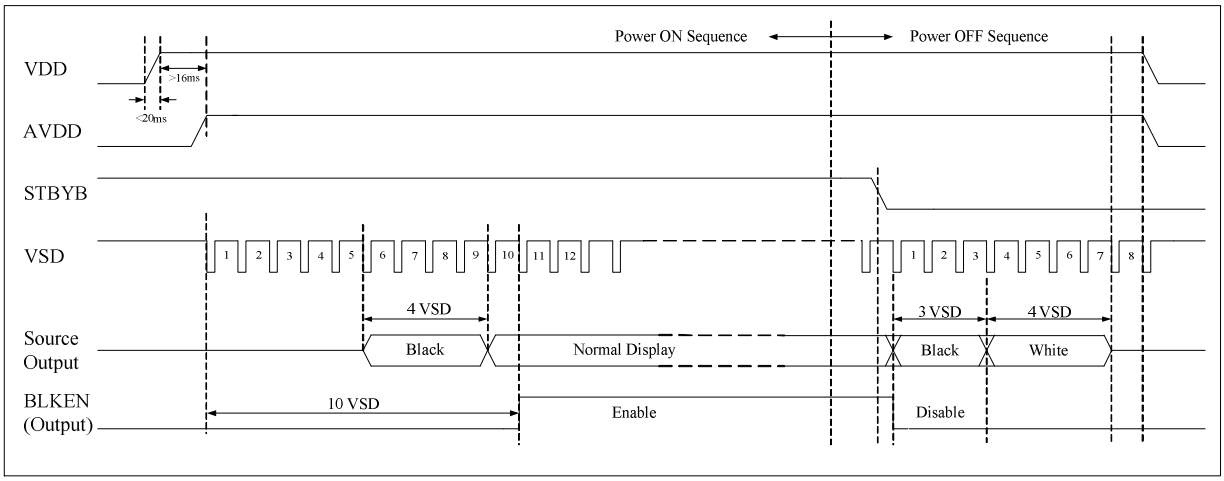
DATR [17:0]	DBGATE="1" MASL = "1" MASLOC="X"	DBGATE="0" MASL = "1" MASLOC="X" RES[1 :0]="1X"	DBGATE="0" MASL="1" MASLOC="0"	DBGATE="0" MASL="1" MASLOC="1"
Description	Dual Gate Mode	Single Source Mode	tcon+source mode Master locate on panel right side (no cascade; no dual gate)	tcon+source mode Master locate on panel left side (no cascade; no dual gate)
DATR0	X	X	X	X
DATR1	X	X	X	X
DATR2	OEV	OEV	OEV	X
DATR3	X	X	X	X
DATR4	UD	UD	UD	X
DATR5	X	X	X	X
DATR6	CKV	CKV	CKV	X
DATR7	X	X	X	X
DATR8	STV1	STV1	STV1	X
DATR9	X	X	X	X
DATR10	STV2	STV2	STV2	X
DATR11	X	X	X	X
DATR12	STV1	STV1	STV1	X
DATR13	X	X	X	X
DATR14	X	X	X	X
DATR15	X	X	X	X
DATR16	STBN	STBN	X	X
DATR17	X	X	X	X
DCLKR	X	X	X	X
DIOR	X	X	X	X
LDR	X	X	X	X
SYNCR	X	X	X	X

DATR [17:0]	DBGATE="1" MASL = "1" MASLOC="X"	DBGATE="0" MASL = "1" MASLOC="X" RES[1 :0]="1X"	DBGATE="0" MASL="1" MASLOC="0"	DBGATE="0" MASL="1" MASLOC="1"
Description	Dual Gate Mode	Single Source Mode	tcon+source mode Master locate on panel right side (no cascade; no dual gate)	tcon+source mode Master locate on panel left side (no cascade; no dual gate)
DATL0	X	X	X	X
DATL1	X	X	X	X
DATL2	OEV	OEV	X	OEV
DATL3	X	X	X	X
DATL4	UD	UD	X	UD
DATL5	X	X	X	X
DATL6	CKV	CKV	X	CKV
DATL7	X	X	X	X
DATL8	STV1	STV1	X	STV1
DATL9	X	X	X	X
DATL10	STV2	STV2	X	STV2
DATL11	X	X	X	X
DATL12	STV1	STV1	X	STV1
DATL13	X	X	X	X
DATL14	X	X	X	X
DATL15	X	X	X	X
DATL16	STBN	STBN	X	X
DATL17	X	X	X	X
DCLKL	X	X	X	X
DIOL	X	X	X	X
LDL	X	X	X	X
SYNCL	X	X	X	X

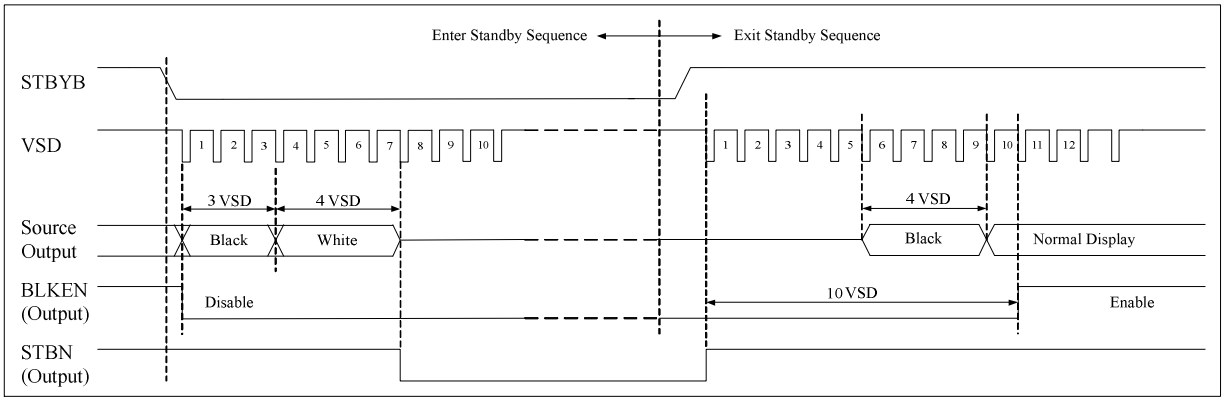
Power On/Off Sequence

In order to prevent IC from power on reset fail, the rising time (TPOR) of the digital power supply VDD should be maintained within the given specifications. Refer to “AC Characteristics” for more detail on timing.

Power-On/Off Timing Sequence



Standby Mode Sequence



Relationship between the Order of Input Data and Output Channels

1. DBGATE="L", Stripe Mode

(1)、SHLR="1" , shift right

Output	SO1	SO2	SO3	- - -	SO1198	SO1199	SO1200
Order	First data			→		Last data	
Odd Line	D07~D00	D17~D10	D27~D20	- - -	D07~D00	D17~D10	D27~D20
Even Line	D07~D00	D17~D10	D27~D20	- - -	D07~D00	D17~D10	D27~D20

(2)、SHLR="0" , shift left

Output	SO1	SO2	SO3	- - -	SO1198	SO1199	SO1200
Order	Last data			←		First data	
Odd Line	D07~D00	D17~D10	D27~D20	- - -	D07~D00	D17~D10	D27~D20
Even Line	D07~D00	D17~D10	D27~D20	- - -	D07~D00	D17~D10	D27~D20

2. DBGATE="H", Stripe Mode

(1)、SHLR="1" , shift right

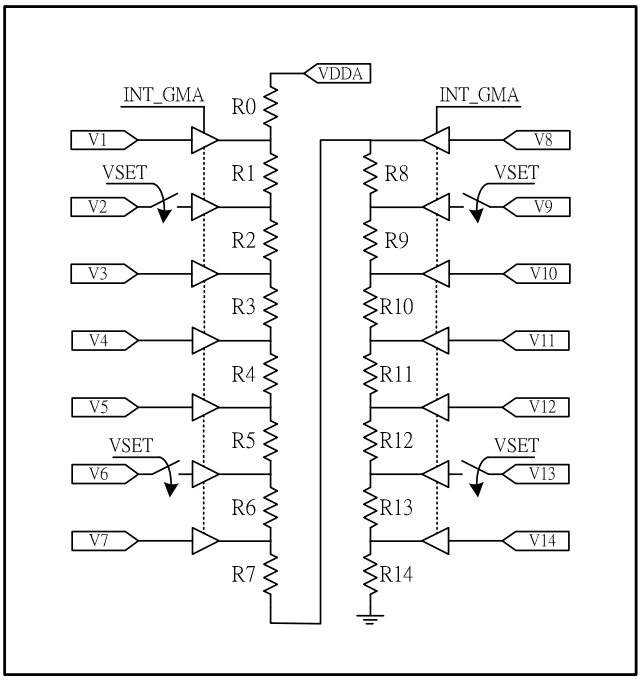
Output	SO1	SO2	SO3	- - -	SO1198	SO1199	SO1200
Order	First data			→		Last data	
Odd Line /Gn	D07~D00	D27~D20	D17~D10	---	D07~D00	D27~D20	D17~D10
Odd Line /Gn+1	D17~D10	D07~D00	D27~D20	---	D17~D10	D07~D00	D27~D20
Even Line /Gn	D07~D00	D27~D20	D17~D10	---	D07~D00	D27~D20	D17~D10
Even Line /Gn+1	D17~D10	D07~D00	D27~D20	---	D17~D10	D07~D00	D27~D20

(2)、SHLR="0" , shift left

Output	SO1	SO2	SO3	- - -	SO1198	SO1199	SO1200
Order	Last data			←		First data	
Odd Line /Gn	D07~D00	D27~D20	D17~D10	---	D07~D00	D27~D20	D17~D10
Odd Line /Gn+1	D17~D10	D07~D00	D27~D20	---	D17~D10	D07~D00	D27~D20
Even Line /Gn	D07~D00	D27~D20	D17~D10	---	D07~D00	D27~D20	D17~D10
Even Line /Gn+1	D17~D10	D07~D00	D27~D20	---	D17~D10	D07~D00	D27~D20

Gamma Adjustment Function

ST5625CA supports gamma voltage generator circuit for V1~V14 gamma correction reference voltage.



Relationship between Input Data and Output Voltage

The figure below shows the relationship between the input data and the output voltage with the output polarity. The range of V1~V7 is for positive polarity, and V8~V14 for negative polarity. Please refer to the next page to get the R-string resistor value and voltage calculation table.

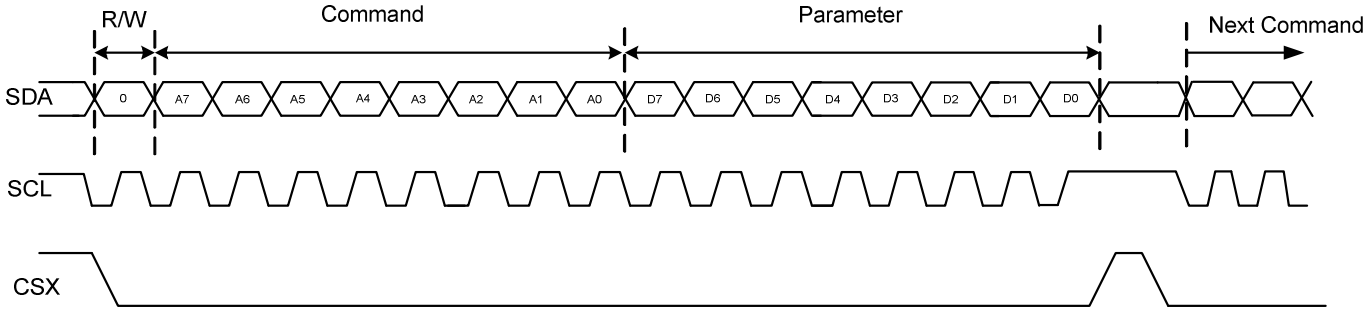
Remark: : AVDD-0.1 ≥ V1 ≥ V2 ≥ V3 ≥ V4≥ V5 ≥ V6 ≥ V7 ; V8 ≥ V9 ≥ V10 ≥ V11 ≥ V12 ≥ V13 ≥ VL14 ≥AGND+0.1V

3-Wire Serial Peripheral Interface (SPI)

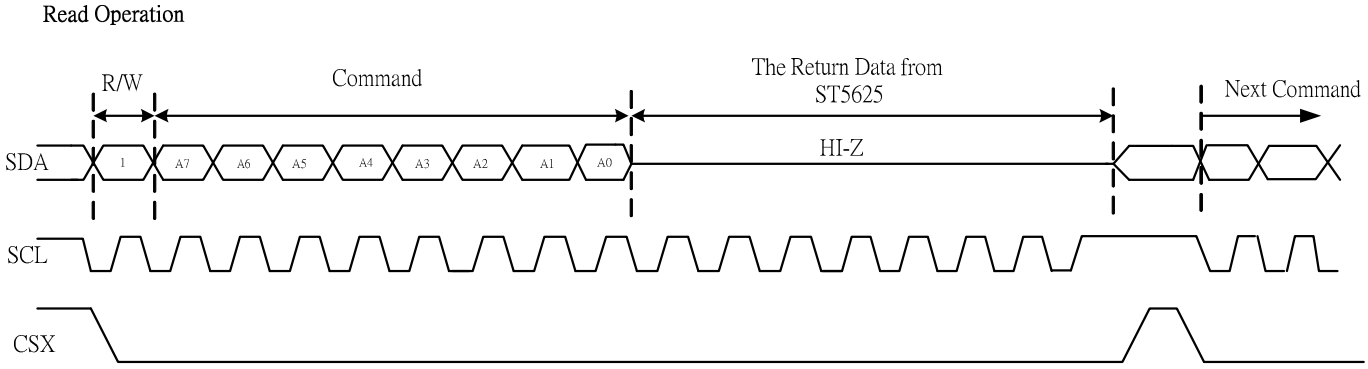
ST5625CA using the 3-line serial port as communication interface for all the commands and parameters. This 3-line serial communication can be bi-directional controlled by the “R/W” bit in address field. Under read mode, the 3-line engine in ST5625CA will return the data during “Data phase”. The returned data should be latched at the rising edge of SCL by external controller. Data in the “Hi-Z phase” will be ignored by 3-line engine during write operation, and should be ignored during read operation also. During read operation, external controller should float SDA pin under “Hi-Z phase” and “Data phase”.
Each Read/Write operation should be exactly 17 bit. To prevent from incorrect setting of the internal register, any write operation with more or less than 17 bit data during a CSX Low period will be ignored by 3-line engine.

The timing diagram of read/write operation is illustrated as below:

Write Operation

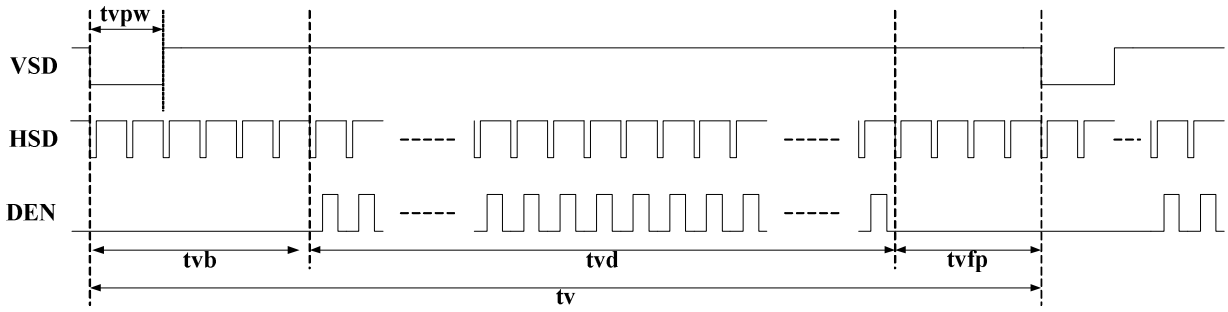


Read Operation

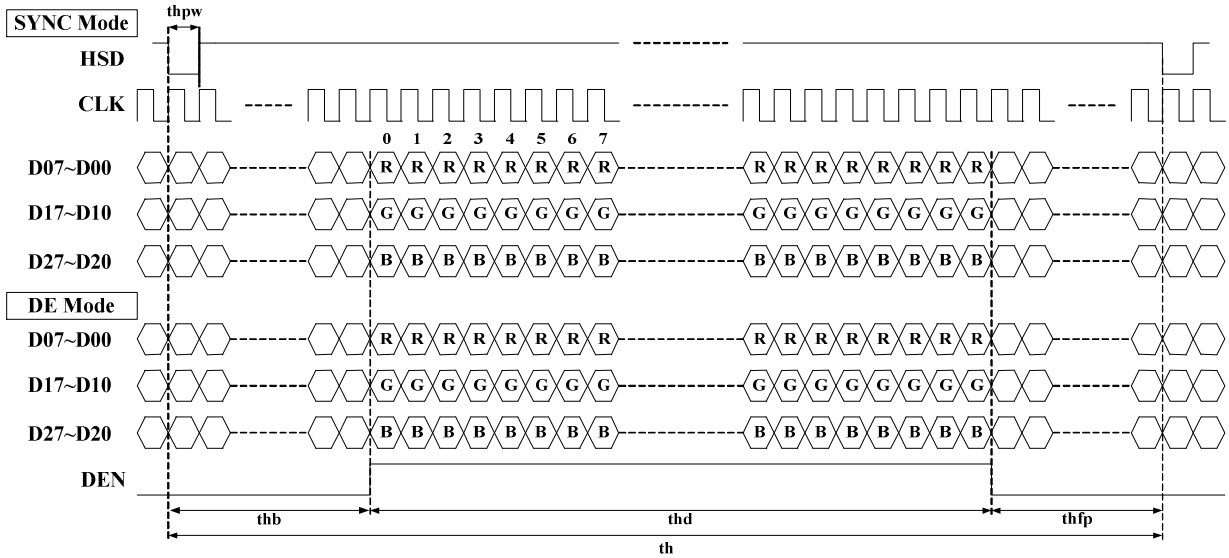


Data Input Format

Vertical input timing



Horizontal input timing



Timing Characteristic

For 800x480 panel

Horizontal input timing

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Horizontal Display Area	thd		800		DCLK
DCLK Frequency	fclk	-	30	50	MHZ
One Horizontal Line	th	889	928	1143	DCLK
HS pulse width	thpw	1	48	255	DCLK
HS Back Porch (Blanking)	thb		88		DCLK
HS Front Porch	thfb	1	40	255	DCLK
DE mode Blanking	th-thd	85	128	512	DCLK

Vertical input timing

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Vertical Display Area	tvd		480		H
VS period time	tv	513	525	767	H
VS pulse width	tvpw	3	3	255	H
VS Back Porch (Blanjing)	tvb		32		H
VS Front Porch	tvfb	1	13	255	H
DE mode Blanking	tv-tvd	4	45	255	H

For 800x600 panel

Horizontal input timing

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Horizontal Display Area	thd		800		DCLK
DCLK Frequency	fclk	-	40	50	MHZ
One Horizontal Line	th	889	1000	1143	DCLK
HS pulse width	thpw	1	48	255	DCLK
HS Back Porch (Blanking)	thb		88		DCLK
HS Front Porch	thfb	1	112	255	DCLK
DE mode Blanking	th-thd	85	200	512	DCLK

Vertical input timing

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Vertical Display Area	tvd		600		H
VS period time	tv	640	600	943	H
VS pulse width	tvpw	3	3	255	H
VS Back Porch (Blanjing)	tvb		39		H
VS Front Porch	tvfb	1	21	255	H
DE mode Blanking	tv-tvd	4	60	255	H

For 640x480 panel

Horizontal input timing

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Horizontal Display Area	thd		640		DCLK
DCLK Frequency	fclk	-	24	50	MHZ
One Horizontal Line	th	-	760	-	DCLK
HS pulse width	thpw	1	48	255	DCLK
HS Back Porch (Blanking)	thb		88		DCLK
HS Front Porch	thfb	1	32	255	DCLK
DE mode Blanking	th-thd	85	120	512	DCLK

Vertical input timing

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Vertical Display Area	tvd		480		H
VS period time	tv	513	525	767	H
VS pulse width	tvpw	3	3	255	H
VS Back Porch (Blanjing)	tvb		32		H
VS Front Porch	tvfb	1	13	255	H
DE mode Blanking	tv-tvd	4	45	255	H

For 400x240 panel

Horizontal input timing

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Horizontal Display Area	thd		400		DCLK
DCLK Frequency	fclk	-	8.4	50	MHZ
One Horizontal Line	th	489	520	743	DCLK
HS pulse width	thpw	1	1	255	DCLK
HS Back Porch (Blanking)	thb		88		DCLK
HS Front Porch	thfb	1	32	255	DCLK
DE mode Blanking	th-thd	85	120	512	DCLK

Vertical input timing

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Vertical Display Area	tvd		240		H
VS period time	tv	258	270	512	H
VS pulse width	tvpw	1	1	255	H
VS Back Porch (Blanjing)	tvb		17		H
VS Front Porch	tvfb	1	13	255	H
DE mode Blanking	tv-tvd	4	30	255	H

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Digital supply voltage	VDD	-0.5 to 5.0	V
Analog supply voltage,	AVDD	-0.5 to 15.0	V
Storage temperature	---	-55 to +125	℃
Operating temperature	---	-20 to +85	℃

CAUTIONS：

Stresses beyond "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operations beyond those indicated under " typical operating conditions" is not implied. Exposure to absolute maximum rating conditions may affect device reliability

Recommended Operating Range

(GND = AGND = 0V, TA = -20 to +85℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Digital supply voltage	VDD	2.7	3.3	3.6	V
Analog supply voltage,	AVDD	6.5	--	13.5	V
Digital input voltage	VIN	0	--	VCC	V

DC Electrical Characteristics (VDD=2.7~3.6V, AVDD=6.5~13.5V, GND=GNDA=0V, TA=-20~85℃)

Parameter	Symbol	Min	Typ.	Max.	Unit	Conditions
Low level input voltage	**Vil**	0	-	0.3xVDD	V	For digital circuit
High level input voltage	**Vih**	0.7xVDD	-	VDD	V	For digital circuit
Input leakage current	**Ii**	-	-	+/-1	uA	For digital circuit
High level output voltage	**Voh**	VDD-0.4	-	-	V	Ioh=-400uA
Low level output voltage	**Vol**	-	-	GND+0.4	V	Iol=+400uA
Pull low/high resistor	**Ri**	200K	250K	300K	Ohm	For the digital input pin@VDD=3.3V
Digital Operation Current	**Idd**	-	8	10	mA	Fclk=50MHz, FLD=48KHz, VDD=3.3V
Digital Stand-by current	**Ist1**	-	10	50	uA	Clock & all functions are stopped
Analog Operation Current	**Idda**	-	10	12	mA	No load Fclk=50Mhz, FLD=48K@AVDD=10.4V
Analog Stand-by Current	**Ist2**	-	10	50	uA	No load. Clock & all functions are stopped
Input Level of V1~V7	**Vref1**	0.4*AVDD	-	AVDD-0.1	V	Gamma correction voltage input
Input Level of V8~V14	**Vref2**	0.1	-	0.6*AVDD	V	Gamma correction voltage input
Output Voltage deviation	**Vod1**	-	+/- 20	+/- 35	mV	Vo=AGND+0.1V~ AGND +0.5V& Vo= AVDD -0.5V~AVDD-0.1V
Output Voltage deviation	**Vod2**	-	+/- 15	+/- 20	mV	Vo=AGND+0.5V~AVDD-0.5V
Output Voltage offset between chips	**Voc**	-	-	+/- 20	mV	Vo=AGND+0.5V~AVDD-0.5V
Dynamic Range of Output	**Vdr**	0.1	-	AVDD-0.1	V	SO1~SO1200
Sinking current of Output	**IOLy**	80	-	-	uA	SO1~SO1200; Vo=0.1V vs. 1.0V, AVDD=13.5V
Driving current of outputs	**IOHy**	80	-	-	uA	SO1~SO1200; Vo=13.4V vs. 12.5V, AVDD=13.5V
Resistance of Gamma Table	**Rg**	0.7*Rn	1.0*Rn	1.3*Rn	ohm	Rn:Internal gamma resistor

AC Electrical Characteristics (VDD =2.7~3.6V, AVDD=6.5~13.5V, GNDA=GND=0V, TA= -20~85℃)

Parameter	Symbol	Min	Typ.	Max.	Unit	Conditions
VDD Power on Slew Rate	**T_{POR}**	-	-	20	ms	From 0V to 90% VDD
RSTB pulse width	**T_{RST}**	50	-	-	us	Clkin=50MHz
CLKIN cycle time	**Tcph**	20			ns	
CLKIN pulse duty	**Tcwh**	40	50	60	%	
VSD setup time	**Tvst**	8	-	-	ns	
VSD hold time	**Tvhd**	8	-	-	ns	
HSD setup time	**Thst**	8	-	-	ns	
HSD hold time	**Thhd**	8	-	-	ns	
Data setup time	**Tdsu**	8	-	-	ns	D[7:0], D1[7:0], D2[7:0] to clkin
Date hold time	**Tdhd**	8	-	-	ns	D[7:0], D1[7:0], D2[7:0] to clkin
DE setup time	**Tesu**	8	-	-	ns	
DE hold time	**Tehd**	8	-	-	ns	
Output stable time	**Tsst**	-	-	6	us	10% to 90% target voltage. CL=120pF, R=10Kohm

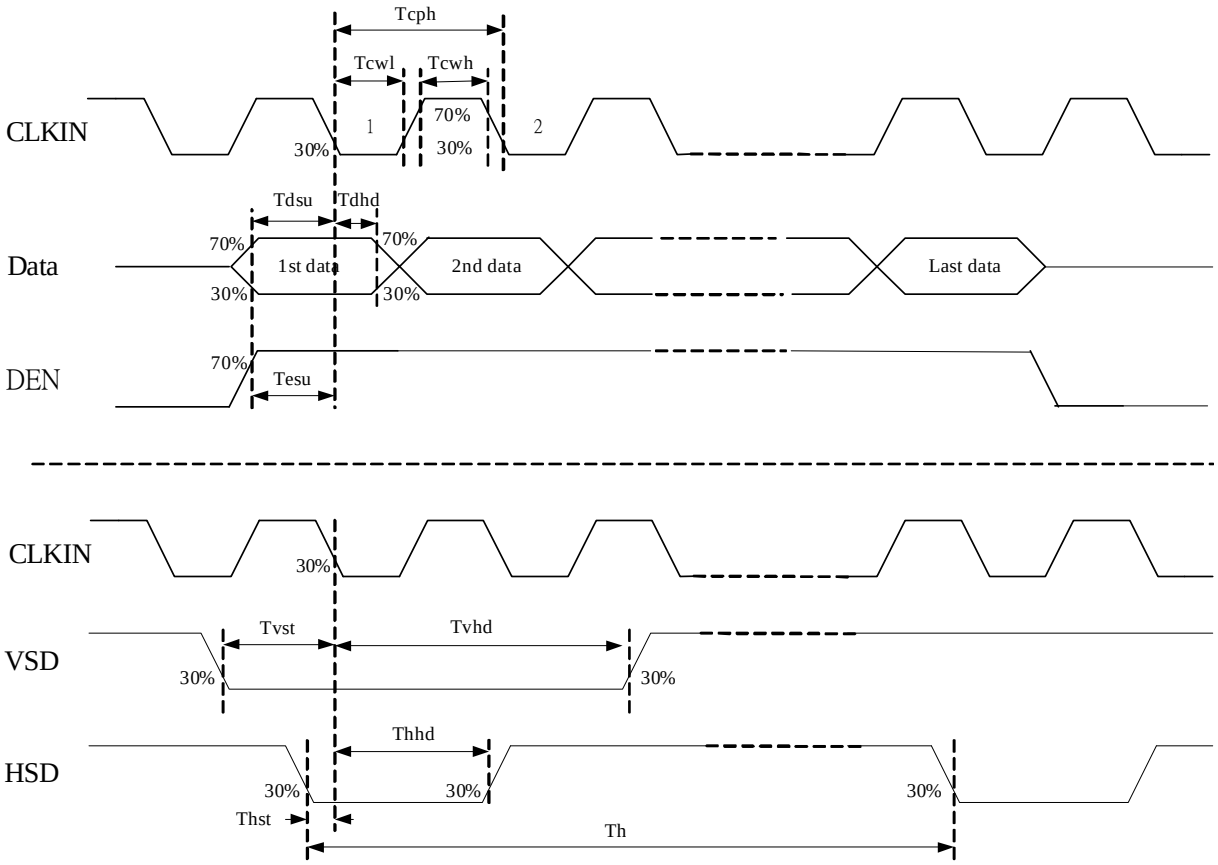
Timing Table

Parallel 24-bit RGB Mode

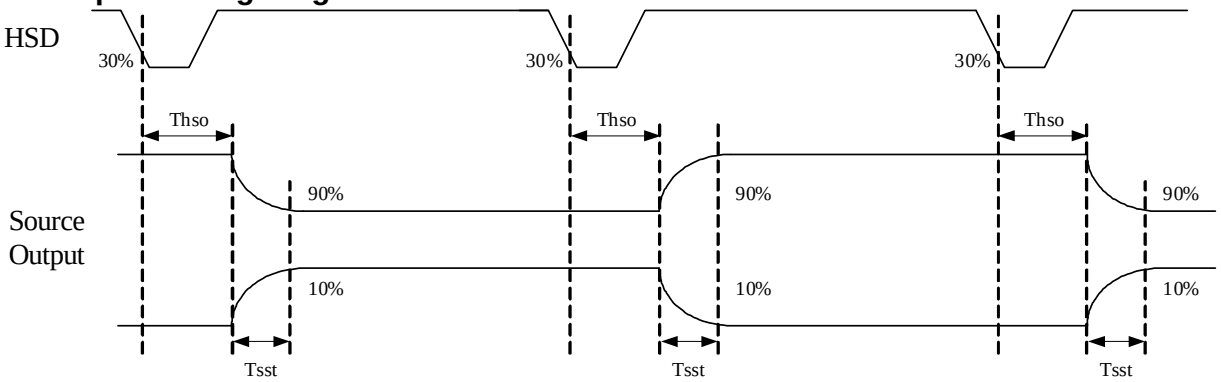
Parameter	Symbol	Min	Typ.	Max.	Unit	Conditions
CLKIN Frequency	Fclk	-	40	50	MHz	VDD=2.7V~3.6V
CLKIN Cycle Time	Tclk	20	25	-	ns	
CLKIN Pulse Duty	Tcwh	40	50	60	%	Tclk
Time from HSD to Source Output	Thso	-	64	-	CLKIN	
Time from HSD to LD	Thld	-	64	-	CLKIN	
Time from HSD to STV	Thstv	-	2	-	CLKIN	
Time from HSD to CKV	Thckv	-	20	-	CLKIN	
Time from HSD to OEV	Thoev	-	4	-	CLKIN	
LD pulse width	Twld	-	10	-	CLKIN	
CKV pulse width	Twckv	-	66	-	CLKIN	
OEV pulse width	Twoev	-	74	-	CLKIN	

Timing Diagram

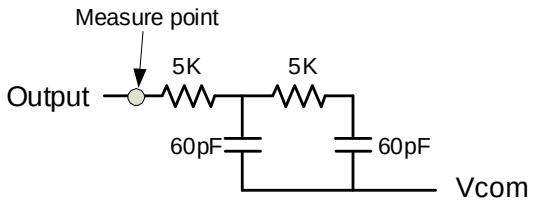
Input Clock and Data Timing Diagram



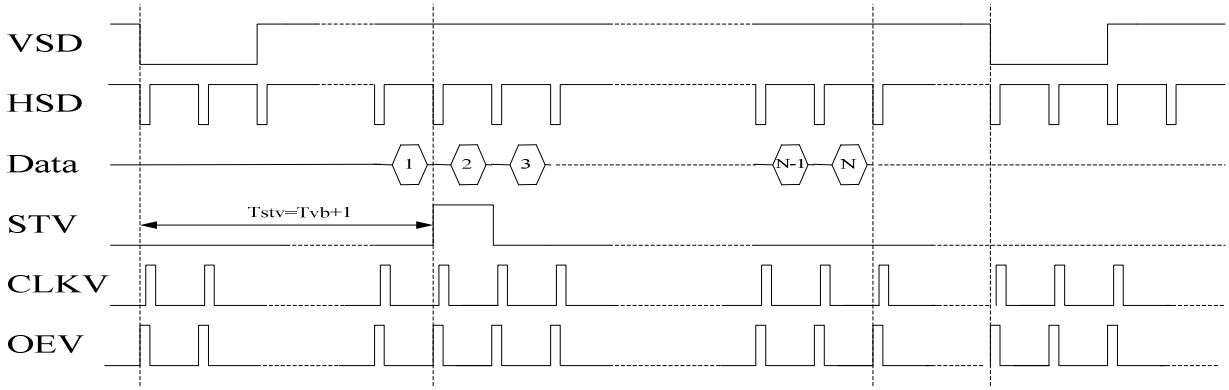
Source Output Timing Diagram



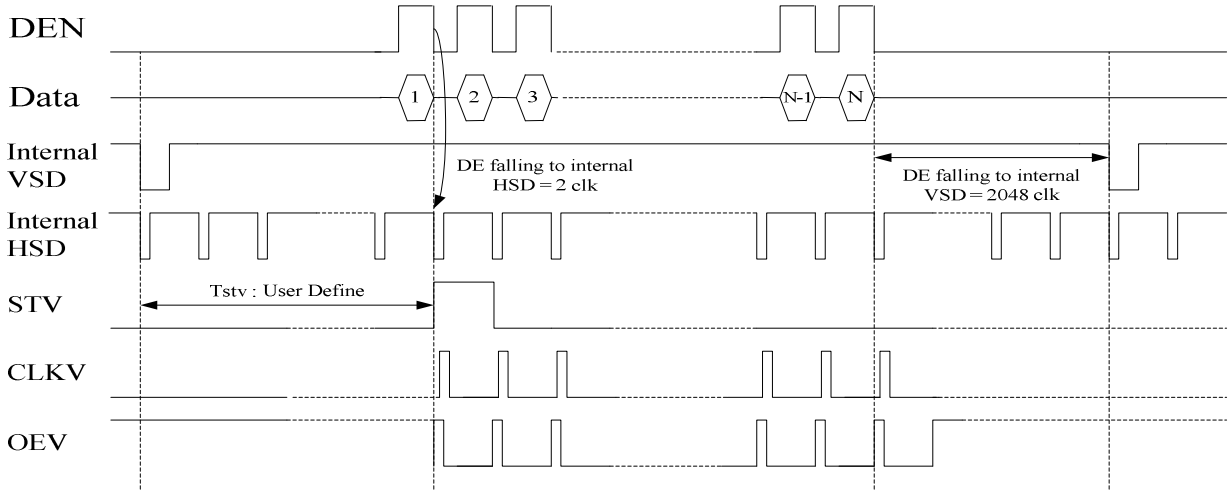
Output Load Condition



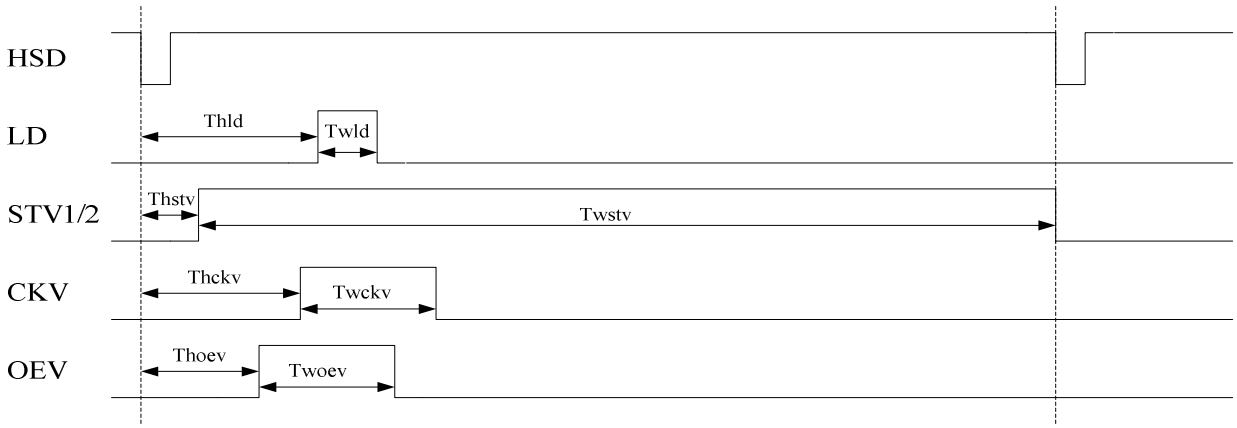
Vertical Timing Diagram SYNC (TCON + Source Mode)



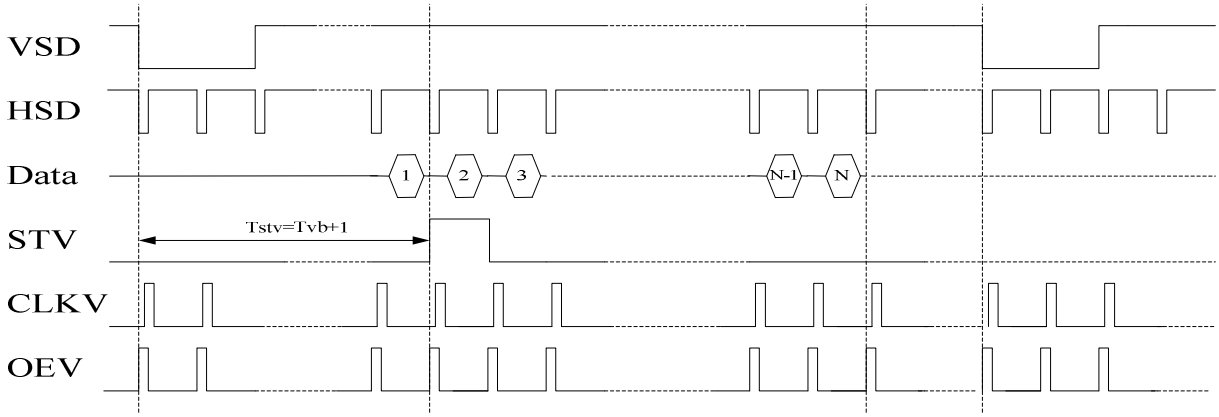
Vertical Timing Diagram DE (TCON + Source Mode)



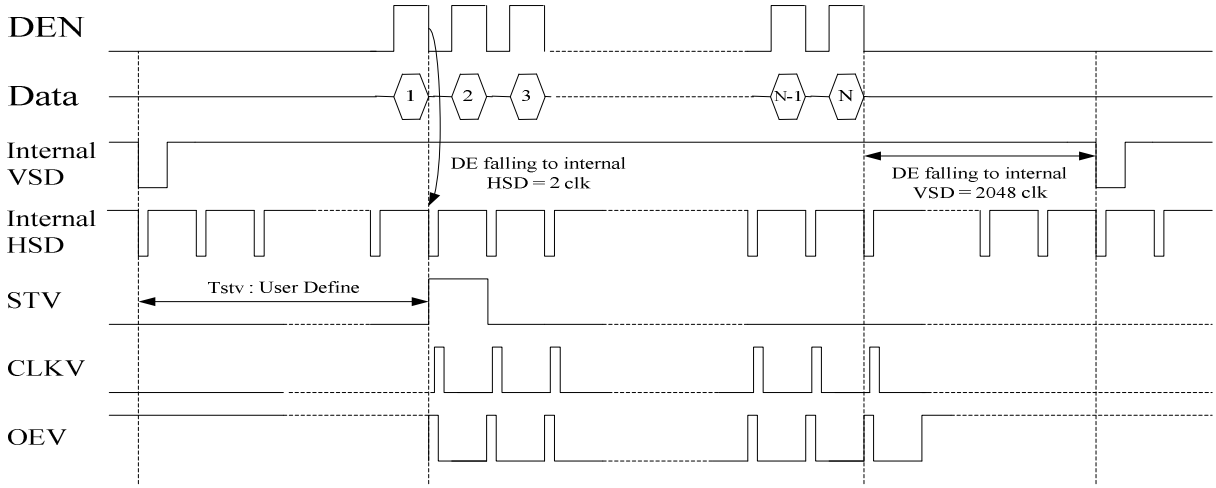
Gate output Timing Diagram (TCON + Source Mode)



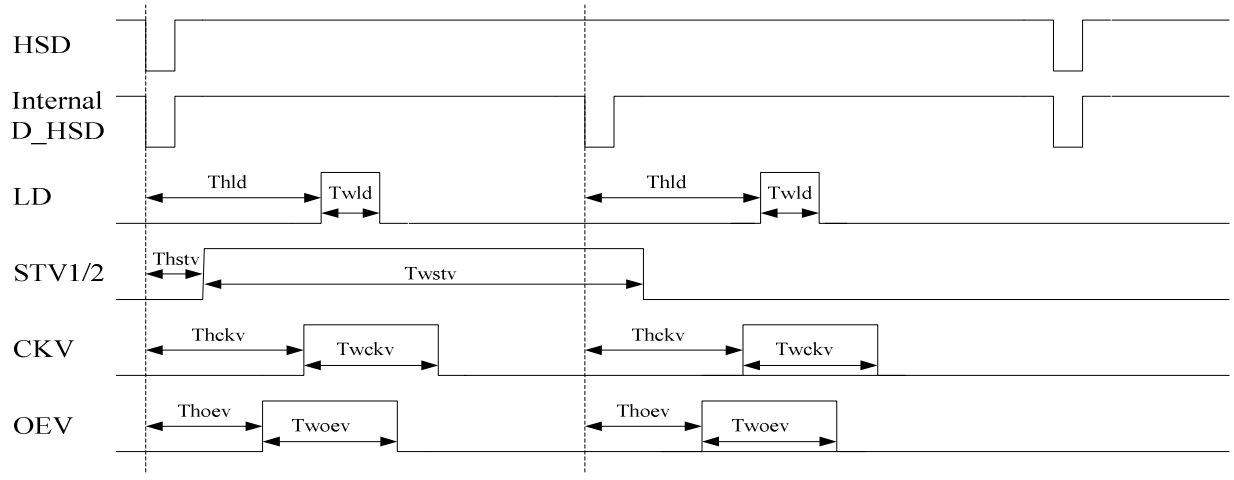
Vertical Timing Diagram SYNC (Dual Gate Mode)



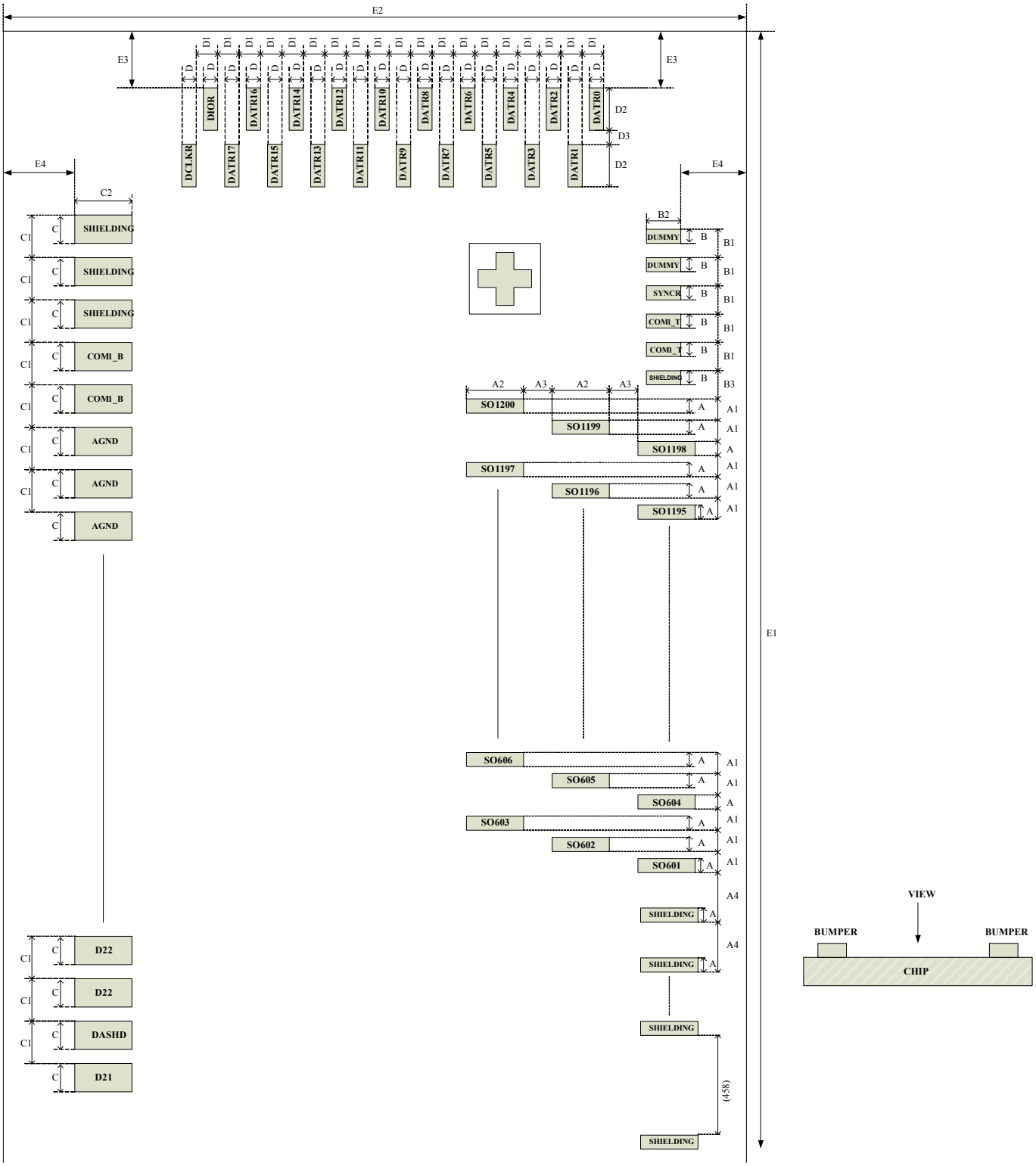
Vertical Timing Diagram DE (Dual Gate Mode)

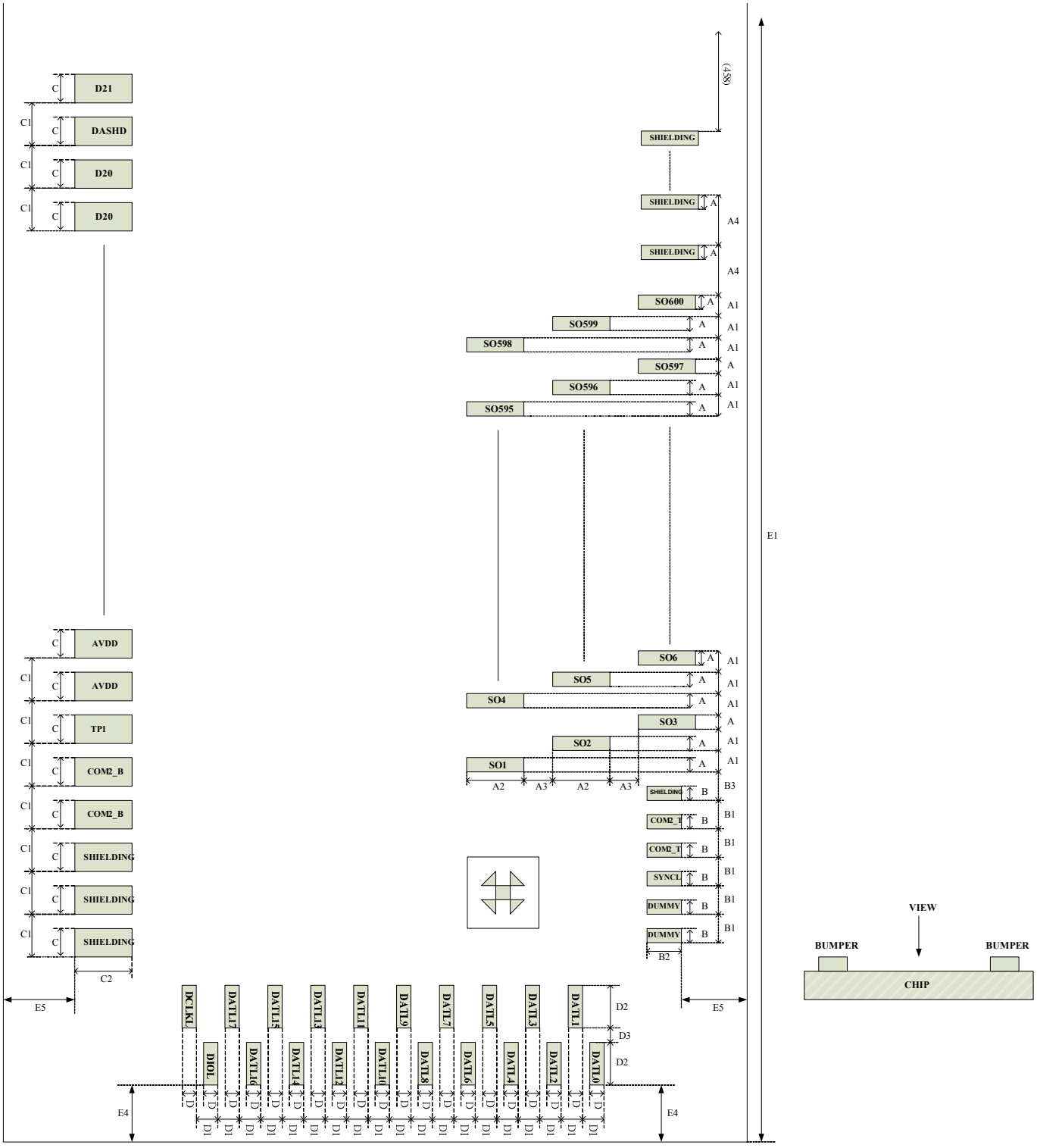


Gate output Timing Diagram (Dual Gate Mode)

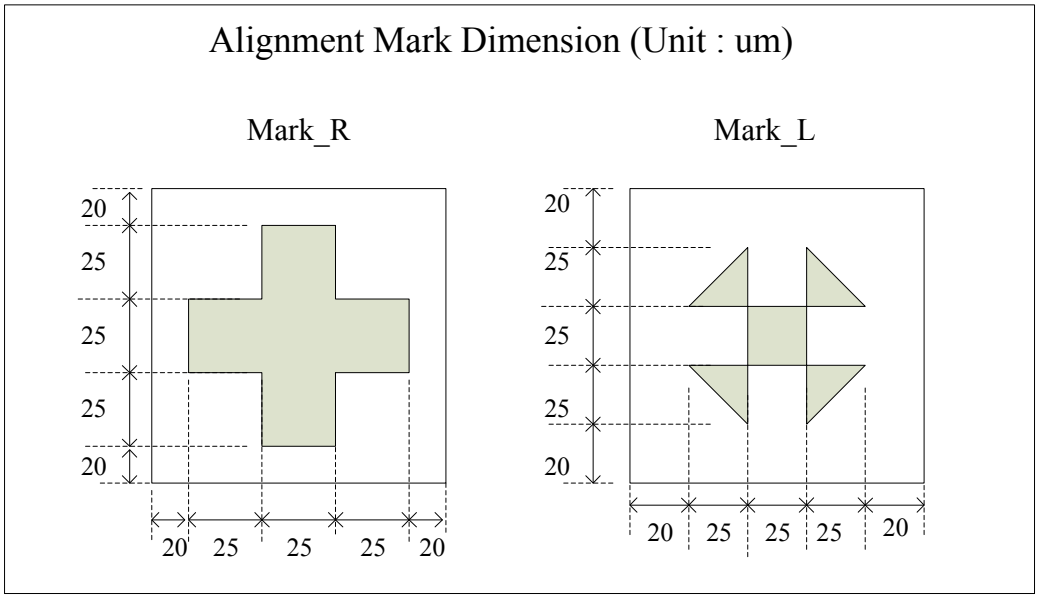


Chip Outline Dimensions (Bump Side)




D21
DASHD
D20
D20
AVDD
AVDD
TP1
COM2_B
COM2_B
SHIELDING
SHIELDING
SHIELDING
SHIELDING
SHIELDING
SO600
SO599
SO598
SO597
SO596
SO595
SO6
SO5
SO4
SO3
SO2
SO1
SHIELDING
COM2_T
COM2_T
SYNCL
DUMMY
DUMMY
DCLKL
DIOL
DATL7
DATL6
DATL5
DATL4
DATL3
DATL2
DATL1
DATL0
DATL9
DATL8
DATL11
DATL10
DATL13
DATL12
DATL15
DATL14
DATL17
DATL16
VIEW
BUMPER
BUMPER
CHIP

Alignment Mark and Pad Dimension



Pad Dimension

Symbol	Dimension (um)
A	17
A1	17
A2	110
A3	30
A4	34
B	30
B1	50
B2	70
B3	50
C	65
C1	85
C2	110

Symbol	Dimension (um)
D	30
D1	40
D2	100
D3	30
E1	22572
E2	938
E3	57
E4	57

Pad Coordinate

No	Name	CX	CY
1	DUMMY	-10922.5	-357
2	DUMMY	-10837.5	-357
3	DUMMY	-10752.5	-357
4	COM1_B	-10667.5	-357
5	COM1_B	-10582.5	-357
6	AGND	-10497.5	-357
7	AGND	-10412.5	-357
8	AGND	-10327.5	-357
9	AGND	-10242.5	-357
10	Dot_POL	-10157.5	-357
11	SHIELDING[2]	-10072.5	-357
12	V1R	-9987.5	-357
13	V1R	-9902.5	-357
14	SHIELDING[3]	-9817.5	-357
15	V2R	-9732.5	-357
16	V2R	-9647.5	-357
17	SHIELDING[4]	-9562.5	-357
18	V3R	-9477.5	-357
19	V3R	-9392.5	-357
20	SHIELDING[5]	-9307.5	-357
21	V4R	-9222.5	-357
22	V4R	-9137.5	-357
23	SHIELDING[6]	-9052.5	-357
24	V5R	-8967.5	-357
25	V5R	-8882.5	-357
26	SHIELDING[7]	-8797.5	-357
27	V6R	-8712.5	-357
28	V6R	-8627.5	-357
29	SHIELDING[8]	-8542.5	-357
30	V7R	-8457.5	-357
31	V7R	-8372.5	-357
32	SHIELDING[9]	-8287.5	-357
33	V8R	-8202.5	-357
34	V8R	-8117.5	-357
35	SHIELDING[10]	-8032.5	-357
36	V9R	-7947.5	-357
37	V9R	-7862.5	-357
38	SHIELDING[11]	-7777.5	-357
39	V10R	-7692.5	-357
40	V10R	-7607.5	-357
41	SHIELDING[12]	-7522.5	-357
42	V11R	-7437.5	-357
43	V11R	-7352.5	-357
44	SHIELDING[13]	-7267.5	-357
45	V12R	-7182.5	-357
46	V12R	-7097.5	-357
47	SHIELDING[14]	-7012.5	-357
48	V13R	-6927.5	-357
49	V13R	-6842.5	-357
50	SHIELDING[15]	-6757.5	-357
51	V14R	-6672.5	-357
52	V14R	-6587.5	-357
53	SHIELDING[16]	-6502.5	-357
54	EXT_VSET	-6417.5	-357
55	TP0	-6332.5	-357
56	TP4	-6247.5	-357
57	DUMMY	-6162.5	-357
58	DUMMY	-6077.5	-357
59	REV	-5992.5	-357
60	BIST	-5907.5	-357
61	BIST	-5822.5	-357
62	INVZ	-5737.5	-357
63	AVDD	-5652.5	-357
64	AVDD	-5567.5	-357
65	AVDD	-5482.5	-357
66	AVDD	-5397.5	-357
67	DUMMY	-5312.5	-357
68	AGND	-5227.5	-357
69	AGND	-5142.5	-357
70	AGND	-5057.5	-357
71	AGND	-4972.5	-357
72	DUMMY	-4887.5	-357
73	GND	-4802.5	-357
74	GND	-4717.5	-357
75	GND	-4632.5	-357
76	GND	-4547.5	-357
77	DUMMY	-4462.5	-357
78	BLKEN	-4377.5	-357
79	BLKEN	-4292.5	-357
80	SHIELDING[25]	-4207.5	-357
81	VDD	-4122.5	-357
82	VDD	-4037.5	-357
83	VDD	-3952.5	-357
84	VDD	-3867.5	-357
85	TP3	-3782.5	-357
86	DBGATE	-3697.5	-357
87	DBGATE	-3612.5	-357
88	CSX	-3527.5	-357
89	MASL	-3442.5	-357
90	DUMMY	-3357.5	-357
91	SCL / DBCM[0]	-3272.5	-357
92	MASLOC	-3187.5	-357
93	MASLOC	-3102.5	-357
94	SDA / DBCM[1]	-3017.5	-357
95	RES[0]	-2932.5	-357
96	RES[0]	-2847.5	-357
97	GMA_SEL	-2762.5	-357
98	COLOR_ENB	-2677.5	-357
99	RES[1]	-2592.5	-357
100	RES[1]	-2507.5	-357
101	PINCTL	-2422.5	-357
102	PINCTL	-2337.5	-357
103	DUMMY	-2252.5	-357
104	VSD	-2167.5	-357
105	VSD	-2082.5	-357
106	DASHD[2]	-1997.5	-357
107	HSD	-1912.5	-357
108	HSD	-1827.5	-357
109	DASHD[3]	-1742.5	-357
110	DEN	-1657.5	-357
111	DEN	-1572.5	-357
112	DASHD[4]	-1487.5	-357
113	CLKIN	-1402.5	-357
114	CLKIN	-1317.5	-357
115	DASHD[5]	-1232.5	-357
116	D2[7]	-1147.5	-357
117	D2[7]	-1062.5	-357
118	D2[6]	-977.5	-357
119	D2[6]	-892.5	-357
120	DASHD[6]	-807.5	-357
121	D2[5]	-722.5	-357
122	D2[5]	-637.5	-357
123	D2[4]	-552.5	-357
124	D2[4]	-467.5	-357
125	DASHD[7]	-382.5	-357
126	D2[3]	-297.5	-357
127	D2[3]	-212.5	-357
128	D2[2]	-127.5	-357
129	D2[2]	-42.5	-357
130	DASHD[8]	42.5	-357
131	D2[1]	127.5	-357
132	D2[1]	212.5	-357
133	D2[0]	297.5	-357
134	D2[0]	382.5	-357
135	DASHD[9]	467.5	-357
136	D1[7]	552.5	-357
137	D1[7]	637.5	-357
138	D1[6]	722.5	-357
139	D1[6]	807.5	-357
140	DASHD[10]	892.5	-357
141	D1[5]	977.5	-357
142	D1[5]	1062.5	-357
143	D1[4]	1147.5	-357
144	D1[4]	1232.5	-357
145	DASHD[11]	1317.5	-357
146	D1[3]	1402.5	-357
147	D1[3]	1487.5	-357
148	D1[2]	1572.5	-357
149	D1[2]	1657.5	-357
150	DASHD[12]	1742.5	-357

151	D1[1]	1827.5	-357
152	D1[1]	1912.5	-357
153	D1[0]	1997.5	-357
154	D1[0]	2082.5	-357
155	DASHD[13]	2167.5	-357
156	D0[7]	2252.5	-357
157	D0[7]	2337.5	-357
158	D0[6]	2422.5	-357
159	D0[6]	2507.5	-357
160	DASHD[14]	2592.5	-357
161	D0[5]	2677.5	-357
162	D0[5]	2762.5	-357
163	D0[4]	2847.5	-357
164	D0[4]	2932.5	-357
165	DASHD[15]	3017.5	-357
166	D0[3]	3102.5	-357
167	D0[3]	3187.5	-357
168	D0[2]	3272.5	-357
169	D0[2]	3357.5	-357
170	DASHD[16]	3442.5	-357
171	D0[1]	3527.5	-357
172	D0[1]	3612.5	-357
173	D0[0]	3697.5	-357
174	D0[0]	3782.5	-357
175	DASHD[17]	3867.5	-357
176	DUMMY	3952.5	-357
177	MODE	4037.5	-357
178	MODE	4122.5	-357
179	CLKPOL	4207.5	-357
180	CLKPOL	4292.5	-357
181	SHIELDING[32]	4377.5	-357
182	DITHB	4462.5	-357
183	DITHB	4547.5	-357
184	INT_GMA	4632.5	-357
185	SHLR	4717.5	-357
186	SHLR	4802.5	-357
187	DUMMY	4887.5	-357
188	UPDN	4972.5	-357
189	UPDN	5057.5	-357
190	DUMMY	5142.5	-357
191	STBYB	5227.5	-357
192	STBYB	5312.5	-357
193	SHIELDING[36]	5397.5	-357
194	RSTB	5482.5	-357
195	RSTB	5567.5	-357
196	TP2	5652.5	-357
197	VDD	5737.5	-357
198	VDD	5822.5	-357
199	VDD	5907.5	-357
200	VDD	5992.5	-357

201	DUMMY	6077.5	-357
202	GND	6162.5	-357
203	GND	6247.5	-357
204	GND	6332.5	-357
205	GND	6417.5	-357
206	HFRC	6502.5	-357
207	V14L	6587.5	-357
208	V14L	6672.5	-357
209	SHIELDING[38]	6757.5	-357
210	V13L	6842.5	-357
211	V13L	6927.5	-357
212	SHIELDING[39]	7012.5	-357
213	V12L	7097.5	-357
214	V12L	7182.5	-357
215	SHIELDING[40]	7267.5	-357
216	V11L	7352.5	-357
217	V11L	7437.5	-357
218	SHIELDING[41]	7522.5	-357
219	V10L	7607.5	-357
220	V10L	7692.5	-357
221	SHIELDING[42]	7777.5	-357
222	V9L	7862.5	-357
223	V9L	7947.5	-357
224	SHIELDING[43]	8032.5	-357
225	V8L	8117.5	-357
226	V8L	8202.5	-357
227	SHIELDING[44]	8287.5	-357
228	V7L	8372.5	-357
229	V7L	8457.5	-357
230	SHIELDING[45]	8542.5	-357
231	V6L	8627.5	-357
232	V6L	8712.5	-357
233	SHIELDING[46]	8797.5	-357
234	V5L	8882.5	-357
235	V5L	8967.5	-357
236	SHIELDING[47]	9052.5	-357
237	V4L	9137.5	-357
238	V4L	9222.5	-357
239	SHIELDING[48]	9307.5	-357
240	V3L	9392.5	-357
241	V3L	9477.5	-357
242	SHIELDING[49]	9562.5	-357
243	V2L	9647.5	-357
244	V2L	9732.5	-357
245	SHIELDING[50]	9817.5	-357
246	V1L	9902.5	-357
247	V1L	9987.5	-357
248	SHIELDING[51]	10072.5	-357
249	AVDD	10157.5	-357
250	AVDD	10242.5	-357

251	AVDD	10327.5	-357
252	AVDD	10412.5	-357
253	TP1	10497.5	-357
254	COM2_B	10582.5	-357
255	COM2_B	10667.5	-357
256	DUMMY	10752.5	-357
257	DUMMY	10837.5	-357
258	DUMMY	10922.5	-357
259	DCLKL	11049	-363
260	DIOL	11179	-323
261	DATL[17]	11049	-283
262	DATL[16]	11179	-243
263	DATL[15]	11049	-203
264	DATL[14]	11179	-163
265	DATL[13]	11049	-123
266	DATL[12]	11179	-83
267	DATL[11]	11049	-43
268	DATL[10]	11179	-3
269	DATL[9]	11049	37
270	DATL[8]	11179	77
271	DATL[7]	11049	117
272	DATL[6]	11179	157
273	DATL[5]	11049	197
274	DATL[4]	11179	237
275	DATL[3]	11049	277
276	DATL[2]	11179	317
277	DATL[1]	11049	357
278	DATL[0]	11179	397
279	DUMMY	10914	377
280	DUMMY	10864	377
281	SYNCL	10814	377
282	COM2_T	10764	377
283	COM2_T	10714	377
284	SHIELDING[55]	10664	377
285	SO[1]	10620.5	77
286	SO[2]	10603.5	217
287	SO[3]	10586.5	357
288	SO[4]	10569.5	77
289	SO[5]	10552.5	217
290	SO[6]	10535.5	357
291	SO[7]	10518.5	77
292	SO[8]	10501.5	217
293	SO[9]	10484.5	357
294	SO[10]	10467.5	77
295	SO[11]	10450.5	217
296	SO[12]	10433.5	357
297	SO[13]	10416.5	77
298	SO[14]	10399.5	217
299	SO[15]	10382.5	357
300	SO[16]	10365.5	77

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302	SO[18]	10331.5	357
303	SO[19]	10314.5	77
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305	SO[21]	10280.5	357
306	SO[22]	10263.5	77
307	SO[23]	10246.5	217
308	SO[24]	10229.5	357
309	SO[25]	10212.5	77
310	SO[26]	10195.5	217
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315	SO[31]	10110.5	77
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789	SO[505]	2052.5	77
790	SO[506]	2035.5	217
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1282	SO[986]	-6982.5	217
1283	SO[987]	-6999.5	77
1284	SO[988]	-7016.5	357
1285	SO[989]	-7033.5	217
1286	SO[990]	-7050.5	77
1287	SO[991]	-7067.5	357
1288	SO[992]	-7084.5	217
1289	SO[993]	-7101.5	77
1290	SO[994]	-7118.5	357
1291	SO[995]	-7135.5	217
1292	SO[996]	-7152.5	77
1293	SO[997]	-7169.5	357
1294	SO[998]	-7186.5	217
1295	SO[999]	-7203.5	77
1296	SO[1000]	-7220.5	357
1297	SO[1001]	-7237.5	217
1298	SO[1002]	-7254.5	77
1299	SO[1003]	-7271.5	357
1300	SO[1004]	-7288.5	217
1301	SO[1005]	-7305.5	77
1302	SO[1006]	-7322.5	357
1303	SO[1007]	-7339.5	217
1304	SO[1008]	-7356.5	77
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1306	SO[1010]	-7390.5	217
1307	SO[1011]	-7407.5	77
1308	SO[1012]	-7424.5	357
1309	SO[1013]	-7441.5	217
1310	SO[1014]	-7458.5	77
1311	SO[1015]	-7475.5	357
1312	SO[1016]	-7492.5	217
1313	SO[1017]	-7509.5	77
1314	SO[1018]	-7526.5	357
1315	SO[1019]	-7543.5	217
1316	SO[1020]	-7560.5	77
1317	SO[1021]	-7577.5	357
1318	SO[1022]	-7594.5	217
1319	SO[1023]	-7611.5	77
1320	SO[1024]	-7628.5	357
1321	SO[1025]	-7645.5	217
1322	SO[1026]	-7662.5	77
1323	SO[1027]	-7679.5	357
1324	SO[1028]	-7696.5	217
1325	SO[1029]	-7713.5	77
1326	SO[1030]	-7730.5	357
1327	SO[1031]	-7747.5	217
1328	SO[1032]	-7764.5	77
1329	SO[1033]	-7781.5	357
1330	SO[1034]	-7798.5	217
1331	SO[1035]	-7815.5	77
1332	SO[1036]	-7832.5	357
1333	SO[1037]	-7849.5	217
1334	SO[1038]	-7866.5	77
1335	SO[1039]	-7883.5	357
1336	SO[1040]	-7900.5	217
1337	SO[1041]	-7917.5	77
1338	SO[1042]	-7934.5	357
1339	SO[1043]	-7951.5	217
1340	SO[1044]	-7968.5	77
1341	SO[1045]	-7985.5	357
1342	SO[1046]	-8002.5	217
1343	SO[1047]	-8019.5	77
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1348	SO[1052]	-8104.5	217
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1360	SO[1064]	-8308.5	217
1361	SO[1065]	-8325.5	77
1362	SO[1066]	-8342.5	357
1363	SO[1067]	-8359.5	217
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1365	SO[1069]	-8393.5	357
1366	SO[1070]	-8410.5	217
1367	SO[1071]	-8427.5	77
1368	SO[1072]	-8444.5	357
1369	SO[1073]	-8461.5	217
1370	SO[1074]	-8478.5	77
1371	SO[1075]	-8495.5	357
1372	SO[1076]	-8512.5	217
1373	SO[1077]	-8529.5	77
1374	SO[1078]	-8546.5	357
1375	SO[1079]	-8563.5	217
1376	SO[1080]	-8580.5	77
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1390	SO[1094]	-8818.5	217
1391	SO[1095]	-8835.5	77
1392	SO[1096]	-8852.5	357
1393	SO[1097]	-8869.5	217
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1442	SO[1146]	-9702.5	77
1443	SO[1147]	-9719.5	357
1444	SO[1148]	-9736.5	217
1445	SO[1149]	-9753.5	77
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1447	SO[1151]	-9787.5	217
1448	SO[1152]	-9804.5	77
1449	SO[1153]	-9821.5	357
1450	SO[1154]	-9838.5	217
1451	SO[1155]	-9855.5	77
1452	SO[1156]	-9872.5	357
1453	SO[1157]	-9889.5	217
1454	SO[1158]	-9906.5	77
1455	SO[1159]	-9923.5	357
1456	SO[1160]	-9940.5	217
1457	SO[1161]	-9957.5	77
1458	SO[1162]	-9974.5	357
1459	SO[1163]	-9991.5	217
1460	SO[1164]	-10008.5	77
1461	SO[1165]	-10025.5	357
1462	SO[1166]	-10042.5	217
1463	SO[1167]	-10059.5	77
1464	SO[1168]	-10076.5	357
1465	SO[1169]	-10093.5	217
1466	SO[1170]	-10110.5	77
1467	SO[1171]	-10127.5	357
1468	SO[1172]	-10144.5	217
1469	SO[1173]	-10161.5	77
1470	SO[1174]	-10178.5	357
1471	SO[1175]	-10195.5	217
1472	SO[1176]	-10212.5	77
1473	SO[1177]	-10229.5	357
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1475	SO[1179]	-10263.5	77
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1477	SO[1181]	-10297.5	217
1478	SO[1182]	-10314.5	77
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1480	SO[1184]	-10348.5	217
1481	SO[1185]	-10365.5	77
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1485	SO[1189]	-10433.5	357
1486	SO[1190]	-10450.5	217
1487	SO[1191]	-10467.5	77
1488	SO[1192]	-10484.5	357
1489	SO[1193]	-10501.5	217
1490	SO[1194]	-10518.5	77
1491	SO[1195]	-10535.5	357
1492	SO[1196]	-10552.5	217
1493	SO[1197]	-10569.5	77
1494	SO[1198]	-10586.5	357
1495	SO[1199]	-10603.5	217
1496	SO[1200]	-10620.5	77
1497	SHIELDING[68]	-10664	377
1498	COM1_T	-10714	377
1499	COM1_T	-10764	377
1500	SYNCR	-10814	377

1501	DUMMY	-10864	377
1502	DUMMY	-10914	377
1503	DATR[0]	-11179	397
1504	DATR[1]	-11049	357
1505	DATR[2]	-11179	317
1506	DATR[3]	-11049	277
1507	DATR[4]	-11179	237
1508	DATR[5]	-11049	197
1509	DATR[6]	-11179	157
1510	DATR[7]	-11049	117
1511	DATR[8]	-11179	77
1512	DATR[9]	-11049	37
1513	DATR[10]	-11179	-3
1514	DATR[11]	-11049	-43
1515	DATR[12]	-11179	-83
1516	DATR[13]	-11049	-123
1517	DATR[14]	-11179	-163
1518	DATR[15]	-11049	-203
1519	DATR[16]	-11179	-243
1520	DATR[17]	-11049	-283
1521	DIOR	-11179	-323
1522	DCLKR	-11049	-363
1523	MARK_L	10773	93
1524	MARK_R	-10773	93

Application Circuit Diagram

1. Dual Gate Mode

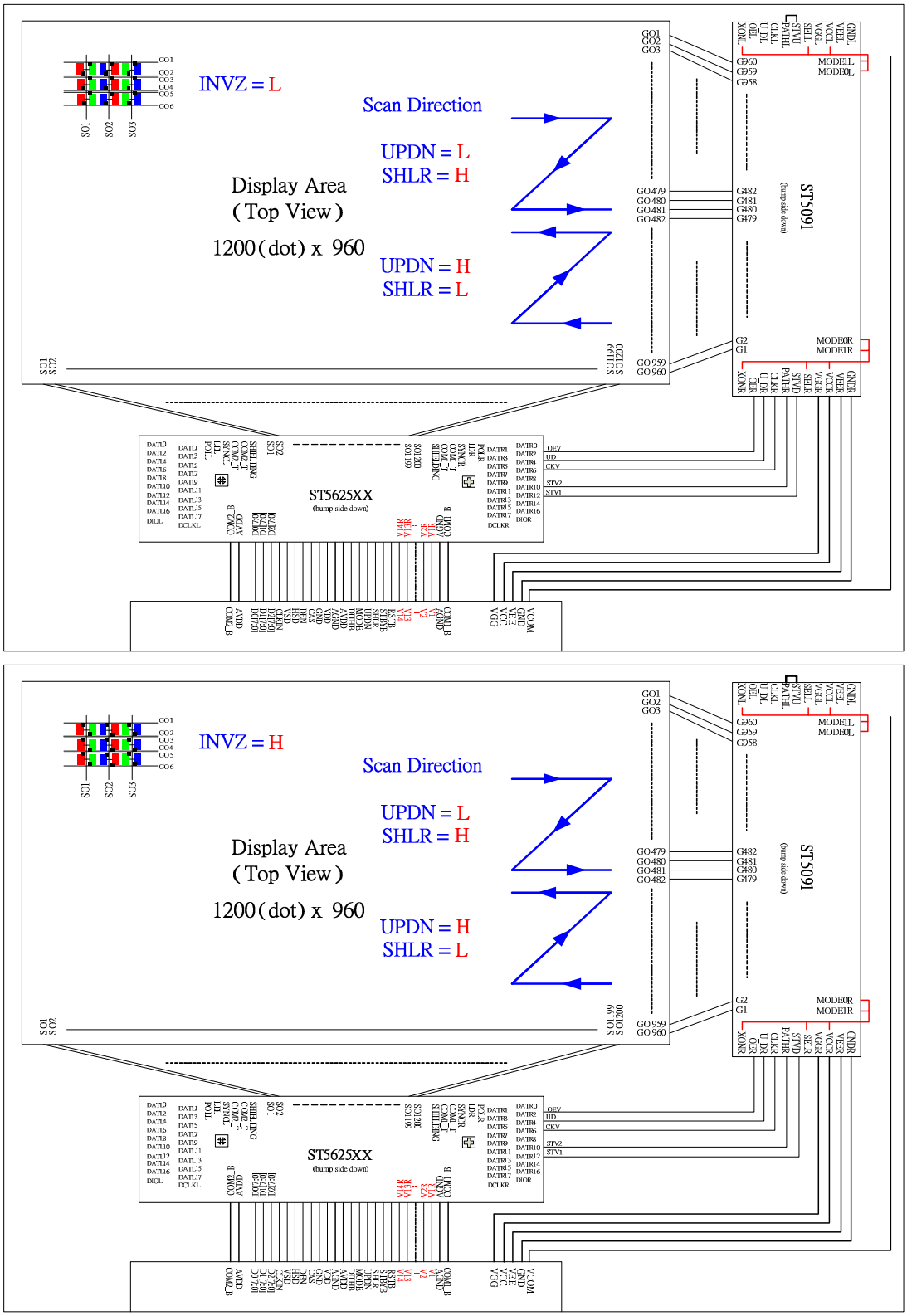
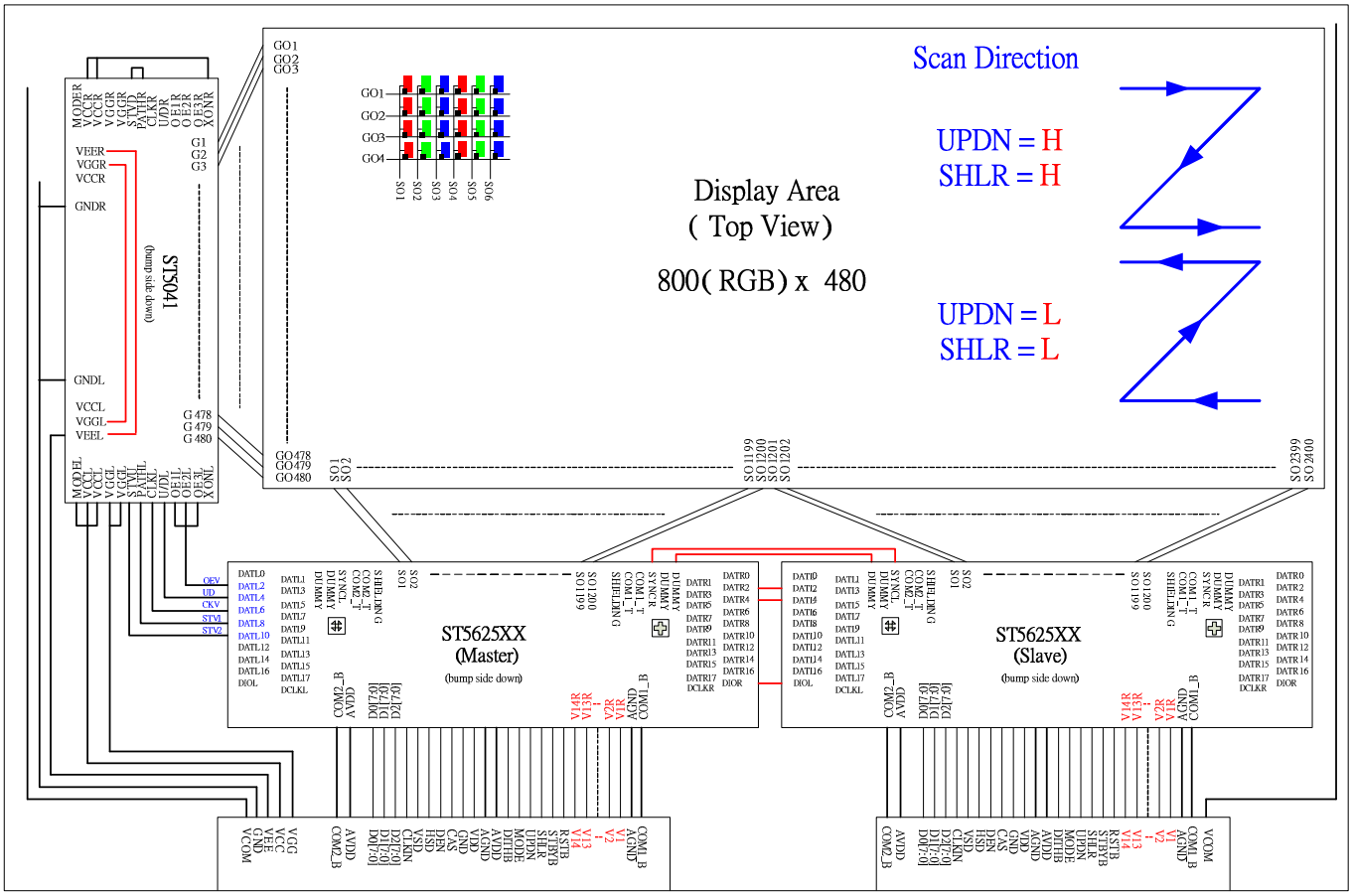


Figure 1 ST5625CA used for Dual Gate Mode

TCON+Source Mode

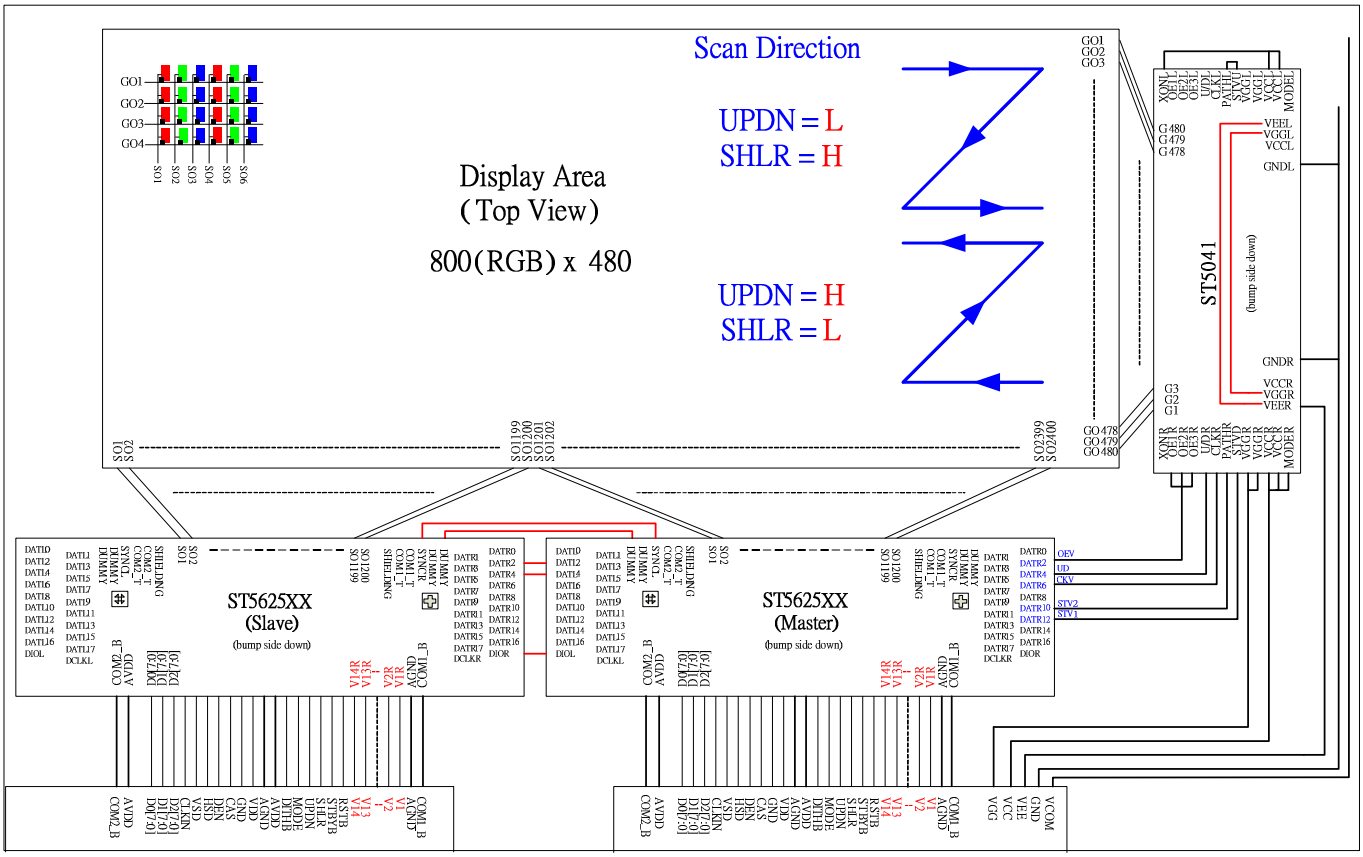


Note : Always use the same side of Gamma correction reference voltage of both ST5625.

Figure 2.1 ST5625CA used for TCON+Source Mode

Master (Left Side)	Slave (Right Side)
RES[1:0] = 00	RES[1:0] = 00
DBGATE = 0	DBGATE = 0
MASL = 1	MASL = 0
MASLOC = 1	MASLOC = 1
MODE = User Define	MODE = User Define
DITHB = User Define	DITHB = User Define
CLKPOL = User Define	CLKPOL = User Define
CFSEL = User Define	CFSEL = User Define
STBYB = User Define	STBYB = User Define
BIST = User Define	BIST = User Define
UPDN = User Define	UPDN = User Define
SHLR = User Define	SHLR = User Define
RSTB = User Define	RSTB = User Define

Table 2.1 Pin Control Setting for Figure 2.1



Note : Always use the same side of Gamma correction reference voltage of both ST5625.

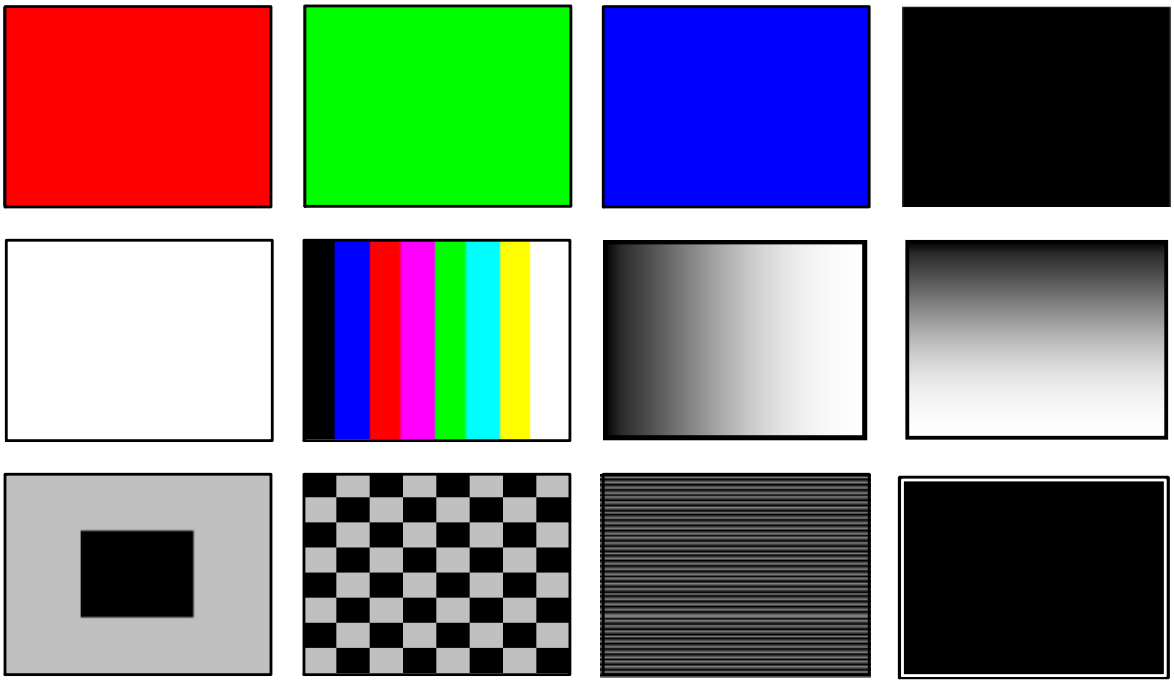
Figure 2.2 ST5625CA used for TCON+Source Mode

Slave (Left Side)	Master (Right Side)
RES[1:0] = 00	RES[1:0] = 00
DBGATE = 0	DBGATE = 0
MASL = 0	MASL = 1
MASLOC = 0	MASLOC = 0
MODE = User Define	MODE = User Define
DITHB = User Define	DITHB = User Define
CLKPOL = User Define	CLKPOL = User Define
CFSEL = User Define	CFSEL = User Define
STBYB = User Define	STBYB = User Define
BIST = User Define	BIST = User Define
UPDN = User Define	UPDN = User Define
SHLR = User Define	SHLR = User Define
RSTB = User Define	RSTB = User Define

Table 2.2 Pin Control Setting for Figure 2.2

BIST Pattern

R -> G -> B -> Black -> White -> Color Bar -> Horizontal 256 gray scale -> Vertical 256 gray scale -> Crosstalk pattern -> Chess board (L255/L0) -> Flicker pattern -> Black background with white out frame



Ordering information

Part.No	Package
ST5625CA – Gx	G : means COG x: means chip thick ness 3 = 400um 4 = 300um

Revision History

Version	Description of Changes	Page	Date
V1.0	First version release		2014/06/12
V1.1	Modify color enhance function control description	7	2014/06/17
V1.2	Modify Application Circuit Diagram of TCON+Source Mode	39,40	2014/07/24
V1.3	Modify Application Circuit Diagram of Dual Gate Mode	38	2014/09/29